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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/680,054	10/05/2000	Shinji Nakamura	0819-430	7323
7590	12/03/2003			
Eric J. Robinson Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22102			EXAMINER KEBEDE, BROOK	
			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/680,054		NAKAMURA ET AL.	
	Examiner		Art Unit	
Brook Kebede		2823		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 08 September 2003.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 17-29,44 and 50-60 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 17-29,44 and 50-60 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____

4) ☐ Interview Summary (PTO-413) Paper No(s). _____

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 17-29 and 44-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsuda et al. (US/6,335,546).

The rejection that was mailed on June 5, 2003 is maintained and repeated herein below as of record.

Re claims 17 and 18, Tsuda et al. disclose a method for the manufacture of a semiconductor device comprising: a step of preparing a substrate (i.e. sapphire substrate) (400) in which a surface (i.e. GaN) therefore is formed a depression (403) having triangle or hexagonal figure (see Fig. 9D) when viewed from the substrate normal; and a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said depression is filled by said semiconductor layer (405) wherein said depression forming step is intentionally performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n) wherein said number n is an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 19, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 20, as applied to claim 19 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression forming step includes step of forming on said major surface of said substrate defined by a (0, 0, 0, 1) plane a depression having a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 21, as applied to claim 17 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 22, as applied to claim 21 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 23, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 24, as applied to claim 23 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 25, as applied to claim 17 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 26, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 27, as applied to claim 25 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 28, as applied to claim 26 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 29, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said substrate preparing step is the step of preparing

Art Unit: 2823

a sapphire substrate on which surface is formed a Group III nitride-based compound semiconductor layer; and wherein said depression forming step is the step of forming said depression in a surface of said Group III nitride-based compound semiconductor layer (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 44, Tsuda et al. disclose a method for the manufacture of a semiconductor substrate including: a step of preparing a substrate (400) for crystal growth; a step of depositing on said crystal growth substrate a first semiconductor layer (402) having a hexagonal crystal structure; a step of exposing either a plane having a plane orientation of $(1, -1, 0, n)$ where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal structure, whereby said plane is covered with semiconductor layer (405) (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 45, as applied to claim 44 above, Tsuda et al. disclose all the limitations including a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and a step of forming a depression by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said depression has an inside face comprising either a plane having a plane orientation of $(1, -1, 0, n)$ where said number n is an arbitrary number, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 46, as applied to claim 45 above, Tsuda et al. disclose all the limitations including the limitation wherein said resist pattern has a plurality of said openings arrayed at equal intervals (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 47, as applied to claim 44 above, Tsuda et al. disclose all the limitations including a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and a step of forming a projection by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said projection has a side face comprising either a plane having a plane orientation of $(1, -1, 0, n)$ where said number n is an arbitrary number or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 48, as applied to claim 47 above, Tsuda et al. disclose all the limitations including the limitation wherein said resist pattern comprises a plurality of said resist patterns arrayed at equal intervals (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 49, Tsuda et al. disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate (i.e. sapphire substrate) (400) in which a surface (i.e. GaN) therefore is formed a depression (403) having triangle or hexagonal figure (see Fig. 9D) when viewed from the substrate normal; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said structure is filled by said semiconductor layer (405); and a step of taking out said semiconductor layer by removal of said substrate, wherein said depression forming step is performed such that an inside face of said depression is intentionally defined by either a plane having a plane orientation of $(1,$

Art Unit: 2823

-1, 0, n) wherein said number n is an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 50, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 51, as applied to claim 18 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said depression has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 52, Tsuda et al. disclose a method for the manufacture of a semiconductor substrate comprising: a step of forming a substrate having on a surface thereof a triangle or hexagonal projection; a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said projection is capped with said semiconductor layer; and a step of taking out said semiconductor layer by removal of said substrate, wherein said projection has a side face intentionally defined by either a plane having a plane orientation of (1, -1, 0, n) wherein said number n is an arbitrary number other than 0, or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 53, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said projection has a side face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 54, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said projection has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 55, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 56, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor (see Figs. 4A – 4D; Col. 4, line 1 – Col. 6, line 33).

Re claim 57, as applied to claim 57 above, Tsuda et al. disclose all the claimed limitations including the limitation wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 58, as applied to claim 56 above, Tsuda et al. disclose all the claimed limitations including the limitation, wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy (see Figs. 9C-9E; Col. 19, line 42 -- Col. 20, line 52).

Re claim 59, as applied to claim 49 above, Tsuda et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a

Art Unit: 2823

sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said depression in a surface thereof (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Re claim 60, as applied to claim 52 above, Tsuda et al. disclose all the claimed limitations including the limitation said substrate forming step including: a step of preparing a sapphire substrate; and a step of forming on said sapphire substrate a Group III nitride-based compound semiconductor layer having said projection on a surface thereof (see Figs. 9C-9E; Col. 19, line 42 – Col. 20, line 52).

Response to Arguments

3. Applicants' arguments filed on March 14, 2003 have been fully considered but they are not persuasive.

Applicants argued that "With respect to the Tsuda et al. reference, this reference merely discloses a GaN semiconductor layer in which a depression formed by etching and a lateral surface of a projection are substantially vertical to the main surface of a substrate. Consequently, the depression and the lateral surface of the projection are defined by a plane orientation of (1, -1, 0, 0), which is clearly different from the plane of orientation of the present invention which is (1, -1, 0, n) where n is not equal to 0. Additionally, as the Examiner can readily appreciate from column 19, lines 16-30, with reference to Fig. 9D, the Tsuda et al. reference cites that the (1, -1, 0, 1) plane is "spontaneously formed." Clearly, such a feature neither discloses nor renders obvious the limitation of Applicants' claimed invention in accordance with Claim 17 that the depression forming step **is intentionally** formed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n) where n is an arbitrary number

Art Unit: 2823

other than 0 or its equivalent plane. Such limitation is also set forth in each of independent claims 18, 49 and 52. Accordingly, in that the Tsuda et al. reference fails to disclose or remotely suggest intentionally forming the depression and the projection having a plane orientation of (1,-1, 0, n) where n is not equal to 0 as set forth in each of independent claims 17, 18, 49 and 52 as well as the fact that the Tsuda et al. reference fails to disclose the step of exposing either a plane having a plane orientation of (1,-1, 0, n) where n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process as recited in independent claim 44. . .”

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989). The Examiner respectfully submits that Tsuda et al. '546 disclose all the claim limitation as applied herein above. For example Tsuda et al. '546 disclose growing a semiconductor layer (i.e., GaN) on (1 -1 0 1) facets. As well-known by ordinary skill in the art this orientation typical hexagonal structure (see Col. 19, lines 44-55. Therefore, applicants contention that “Tsuda also fails to disclose the step of forming on the surface of the substrate a semiconductor layer having a hexagonal crystal structure, whereby the depression is filled by the semiconductor layer” has no merit. In addition, the added element that “intentional” has no patentable weight because

applicant's argument for support "intentional" (i.e., depression forming step **is intentionally** formed) the etching is performed to intentionally form the depression. If that the case, Tsuda et al. '546 disclose all the claim limitation as applied herein above including **intentionally** forming depression (403) having triangle or hexagonal figure (see Fig. 9D). There is no spontaneous process in the formation of depression (403) in Tsuda et al. '546 disclosure, it is formed by etching.

Therefore, the rejection under 35 U.S.C. § 102(e) is deemed proper.

Conclusion

4. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. **After**

Application/Control Number: 09/680,054
Art Unit: 2823

Page 12

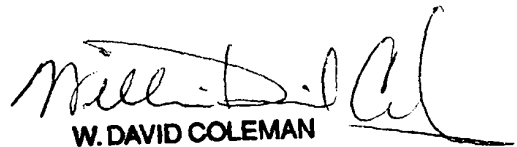
February 4, 2004, the Examiner should be contacted at (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
November 25, 2003


W. DAVID COLEMAN
PRIMARY EXAMINER